EPFL Workshop on Logic Synthesis and Emerging Technologies

Thursday, 28 September 2017

Session: Opening Keynotes

9:00-9:10 **Welcome**
Giovanni De Micheli (*EPFL*)

9:10-9:50 **Some Implications for Logic Synthesis from the Coming Semiconductor Technologies**
Antun Domic (*Synopsys*)

9:50-10:30 **Towards Security without Secrets**
Srini Devadas (*Massachusetts Institute of Technology*)

10:30-11:00 *Coffee break*

Session: Advances in Logic Synthesis

11:00-11:20 **ABC: The Way It Should Have Been Designed**
Alan Mishchenko (*University of California, Berkeley*)

11:20-11:40 **Advances in Industrial Logic Synthesis**
Luca Amaru (*Synopsys*)

11:40-12:00 **The Fascinating Properties of MAJority**
Mathias Soeken (*EPFL*)

12:00-12:30 **Discussion**

12:30-14:00 *Lunch*

Session: In Memory Computing

14:00-14:20 **Logic Synthesis and Automation for Memristive Memory Processing Unit**
Shahar Kvatinsky *(Technion)*

14:20-14:40 **CMOS Compatible 3D Integrated Memristive Memory Array**
Yusuf Leblebici (*EPFL*)

14:40-15:00 **Is It Logic or Memory? - Blurring the Gap**
Vijaykrishnan Narayanan (*Penn State*)

15:00-15:30 **Discussion**

15:30-16:00 *Coffee break*

Session: Tutorials

16:00-16:45 **Ancilla Management for Quantum and Reversible Computation**
Martin Roetteler (*Microsoft*)

16:45-17:30 **BDD/ZDD-based Enumeration Techniques and Real-Life Applications**
Shin-ichi Minato (*Hokkaido University*)

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19:30-22:00 **Gala Dinner**

Friday, 29 September 2017

Session: Approximate Computing and Synthesis

9:00-9:20 **Approximate BDD Optimization**
Rolf Drechsler (*University of Bremen*)

9:20-9:40 **Mapping-aware Logic Synthesis with Parallelized Stochastic Optimization**
Zhiru Zhang (*Cornell University*)

9:40-10:00 **Deep Learning with Low Precision Hardware: Challenges&Opportunities for Logic Synthesis**
Luca Benini (*ETHZ*)

10:00-10:30 **Discussion**

10:30-11:00 *Coffee break*

Session: Design with Functionality-Enhanced Devices

11:00-11:20 **Functionality-Enhanced Devices: An Alternative to Moore's Law**
Pierre-Emmanuel Gaillardon (*University of Utah*)

11:20-11:40 **Synthesis and DSE Techniques for Matrix-based Ambipolar Logic Architectures**
Ian O'Connor (*EC Lyon*)

11:40-12:00 **Logic Synthesis for Reconfigurable Transistors**
Akash Kumar (*TU Dresden*)

12:00-12:30 **Discussion**

12:30-14:00 *Lunch*

Session: Novel Computing Paradigms

14:00-14:20 **Computation with Structured and Unstructured Networks of Emerging Devices**
Christof Teuscher (*Portland State University*)

14:20-14:40 **Silicon Scaling by Exploiting the 3rd Dimension**
Julien Ryckaert (*imec*)

14:40-15:00 **Bringing Technology Information into Early Steps of Logic Synthesis**
Andre Inacio Reis (*UFRGS, Brazil*)

15:00-15:30 **Discussion**

15:30-16:00 *Coffee break*

Session: Closing Keynote

16:00-16:40 **Logic Synthesis of Recombinase-based Genetic Circuits**
Jie-Hong Roland Jiang (*National Taiwan University*)